

FIG. 1

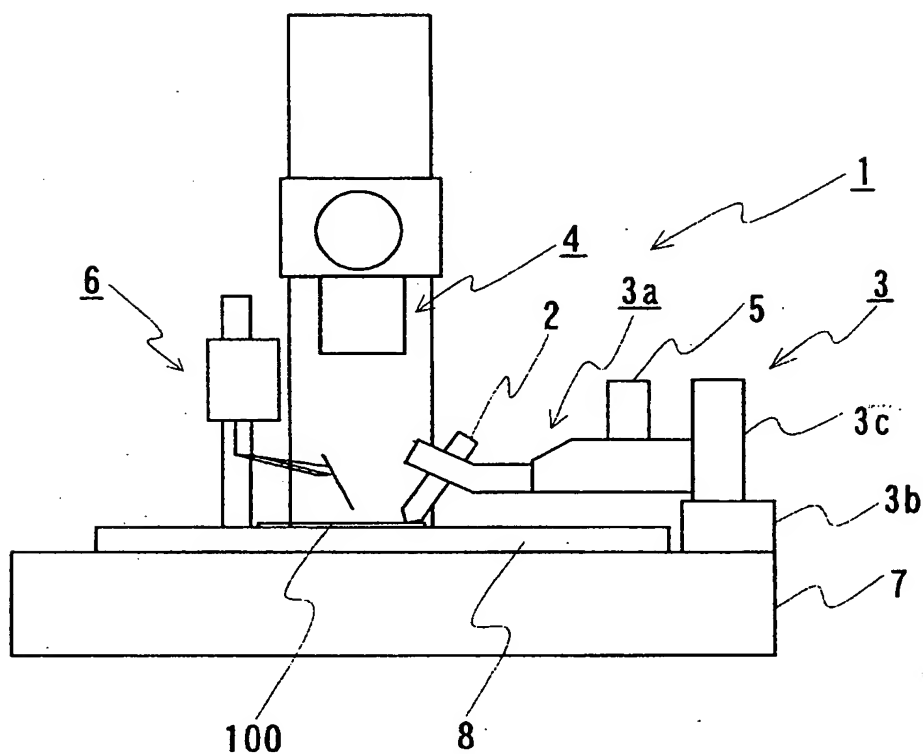


FIG. 2 (A)

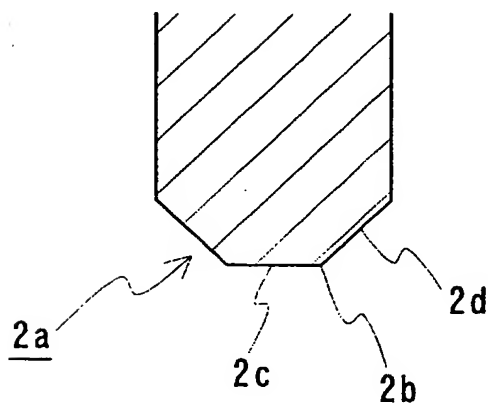


FIG. 2 (B)

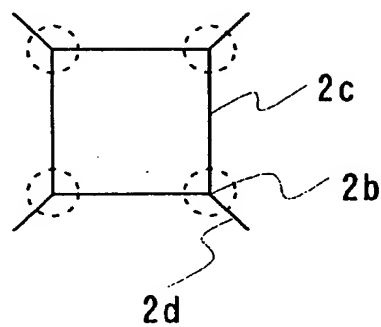


FIG. 3

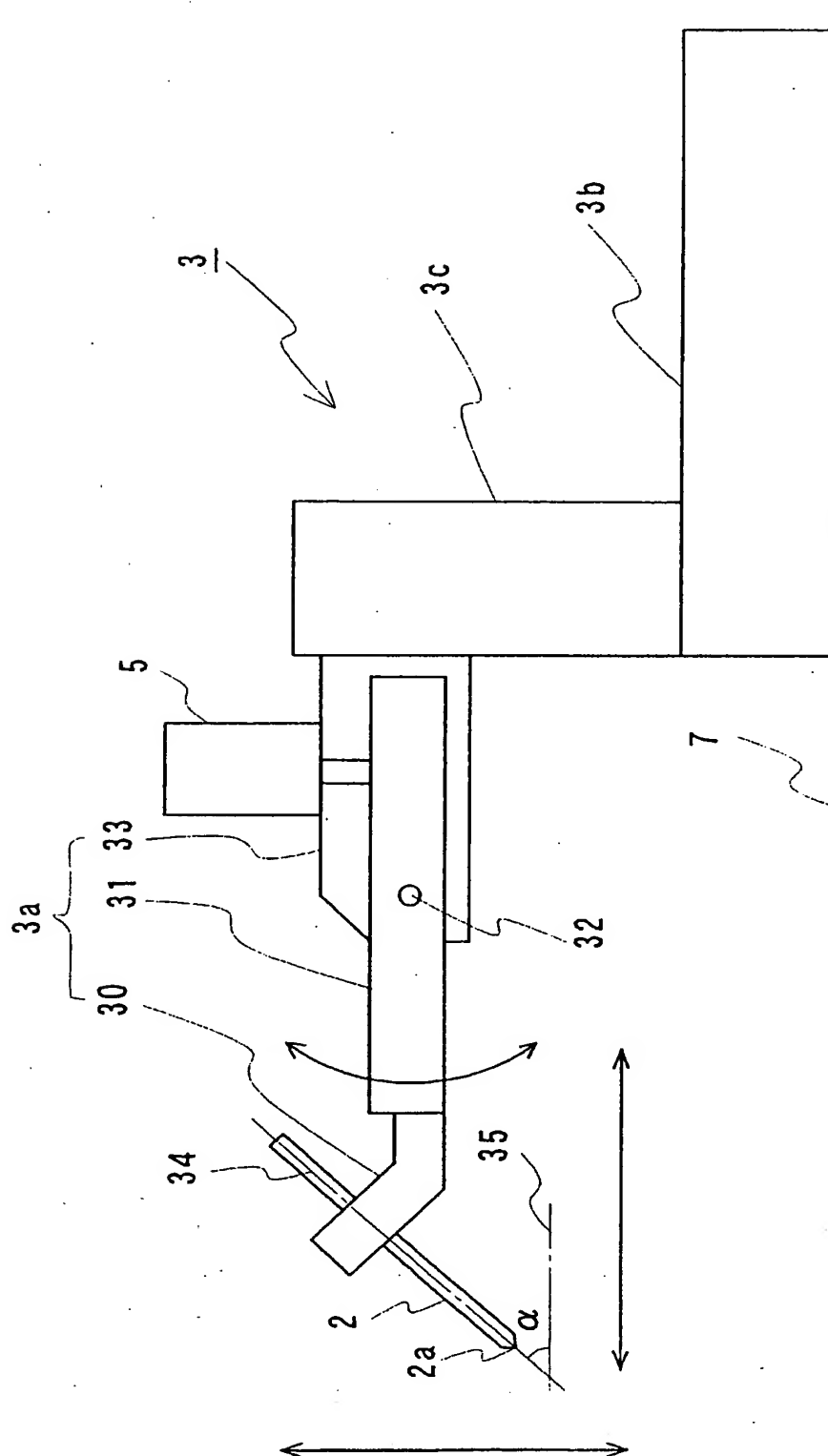


FIG. 4

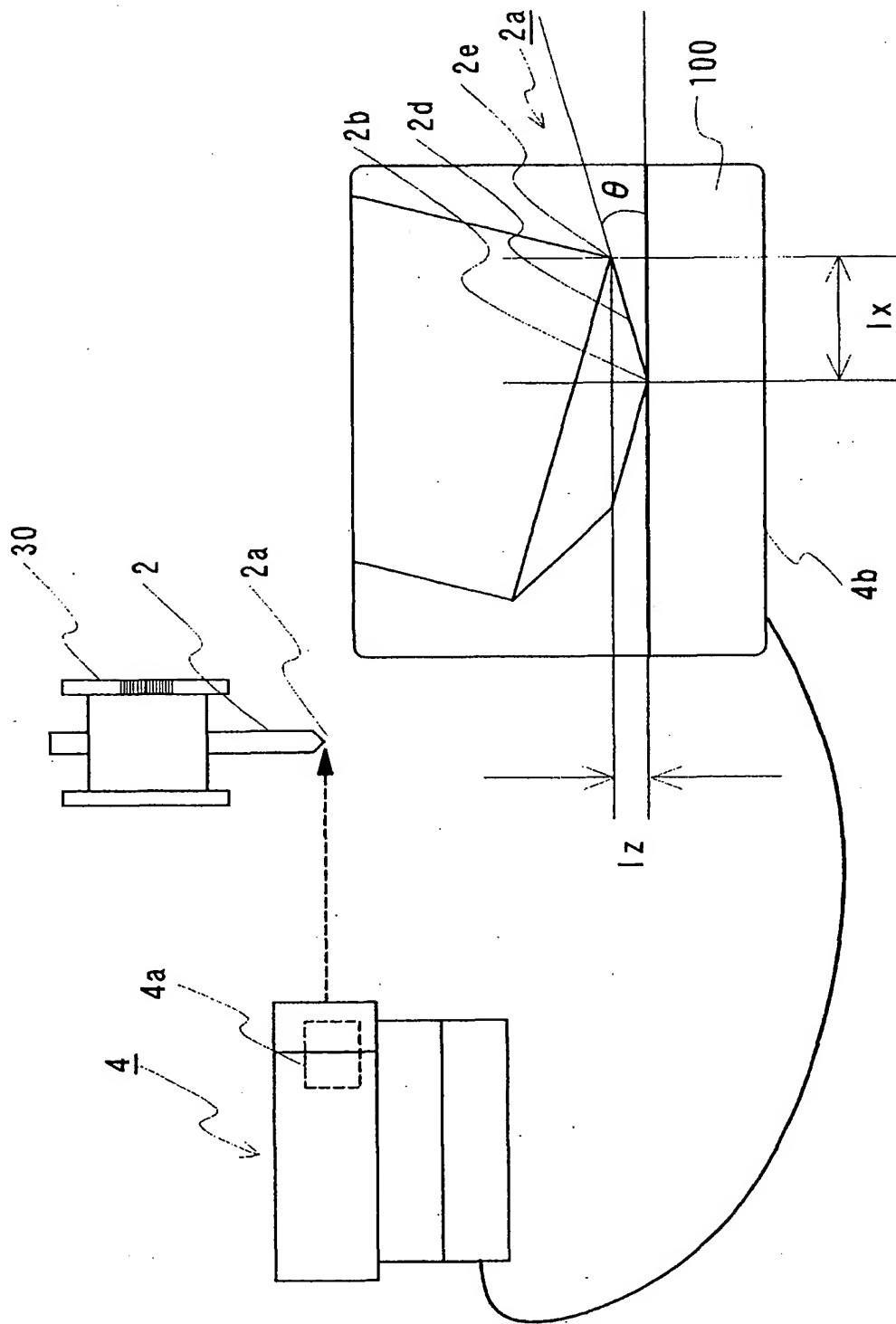


FIG. 6

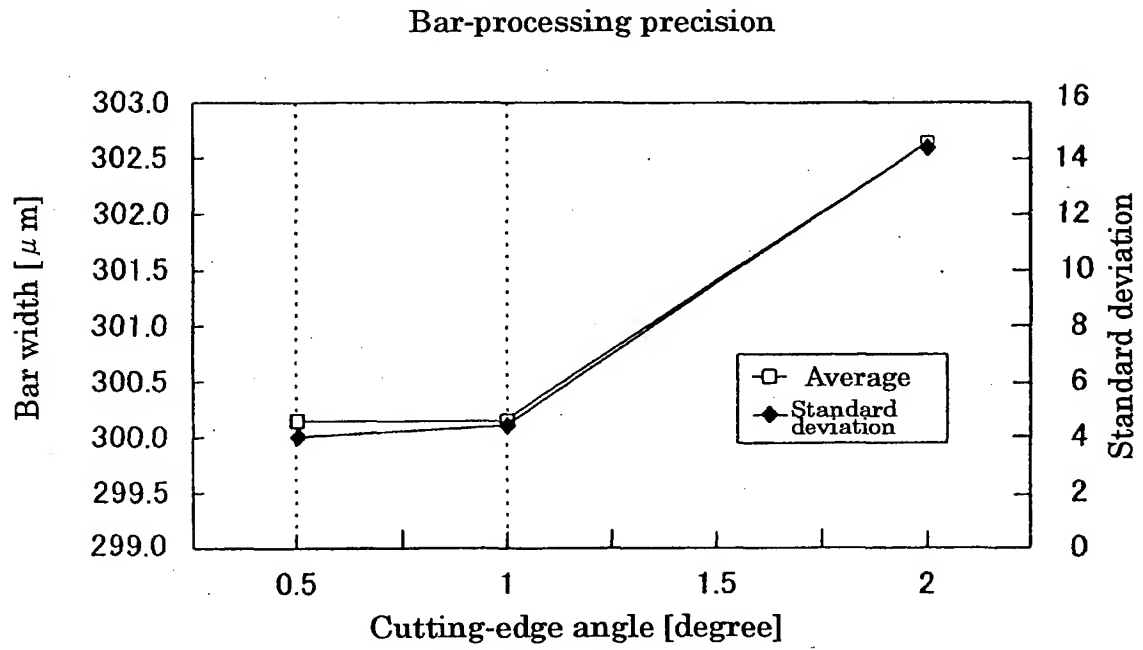


FIG. 7

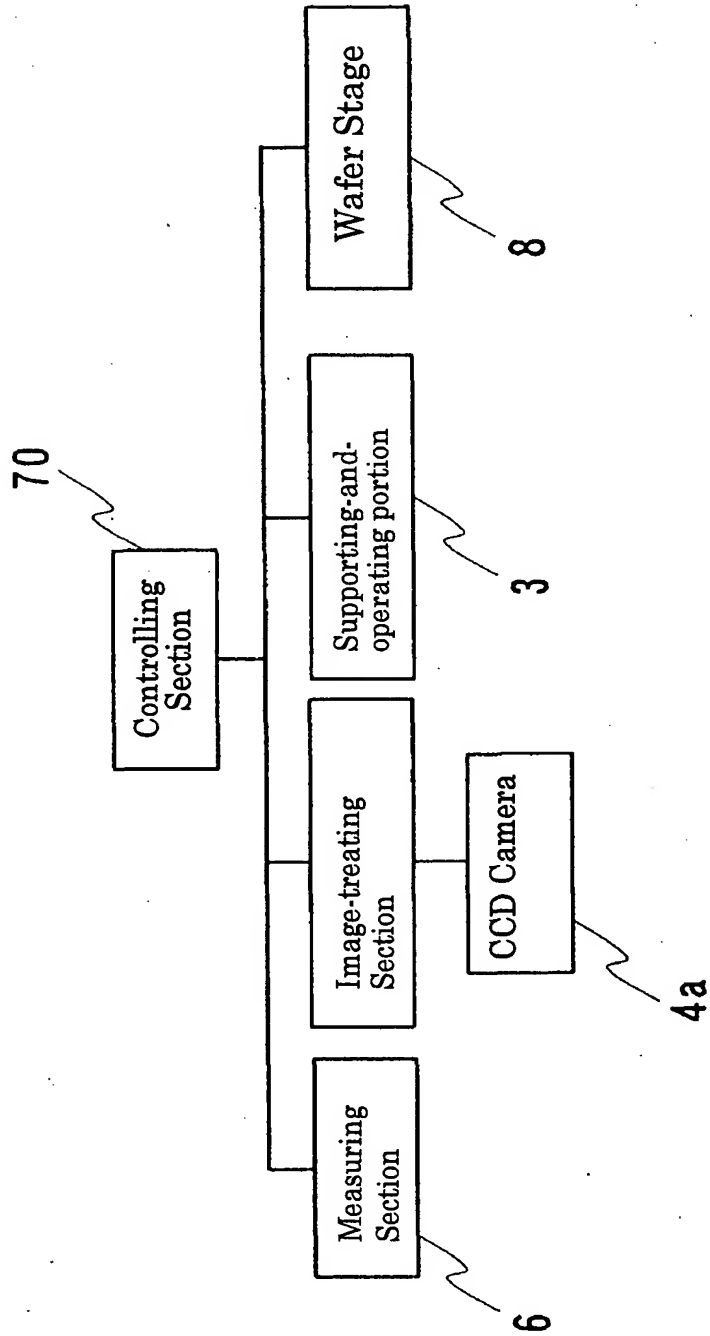


FIG. 8

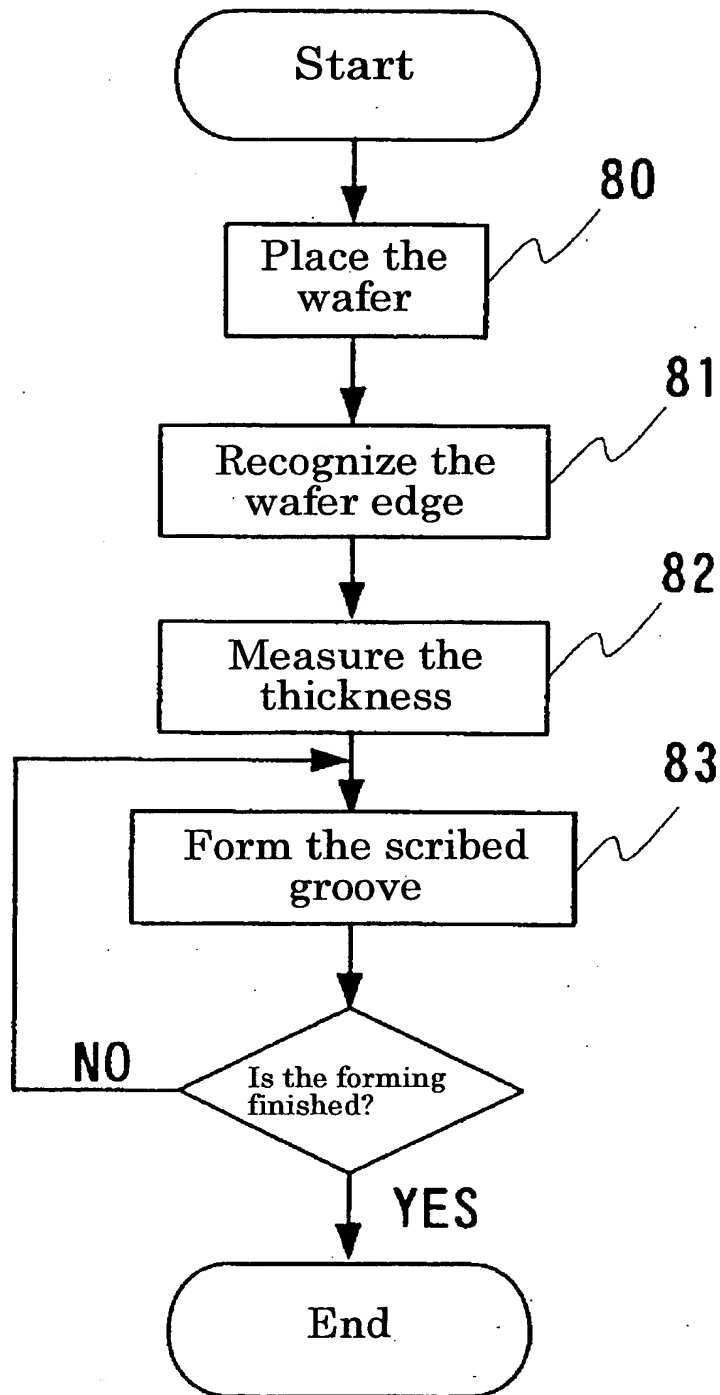


FIG. 9

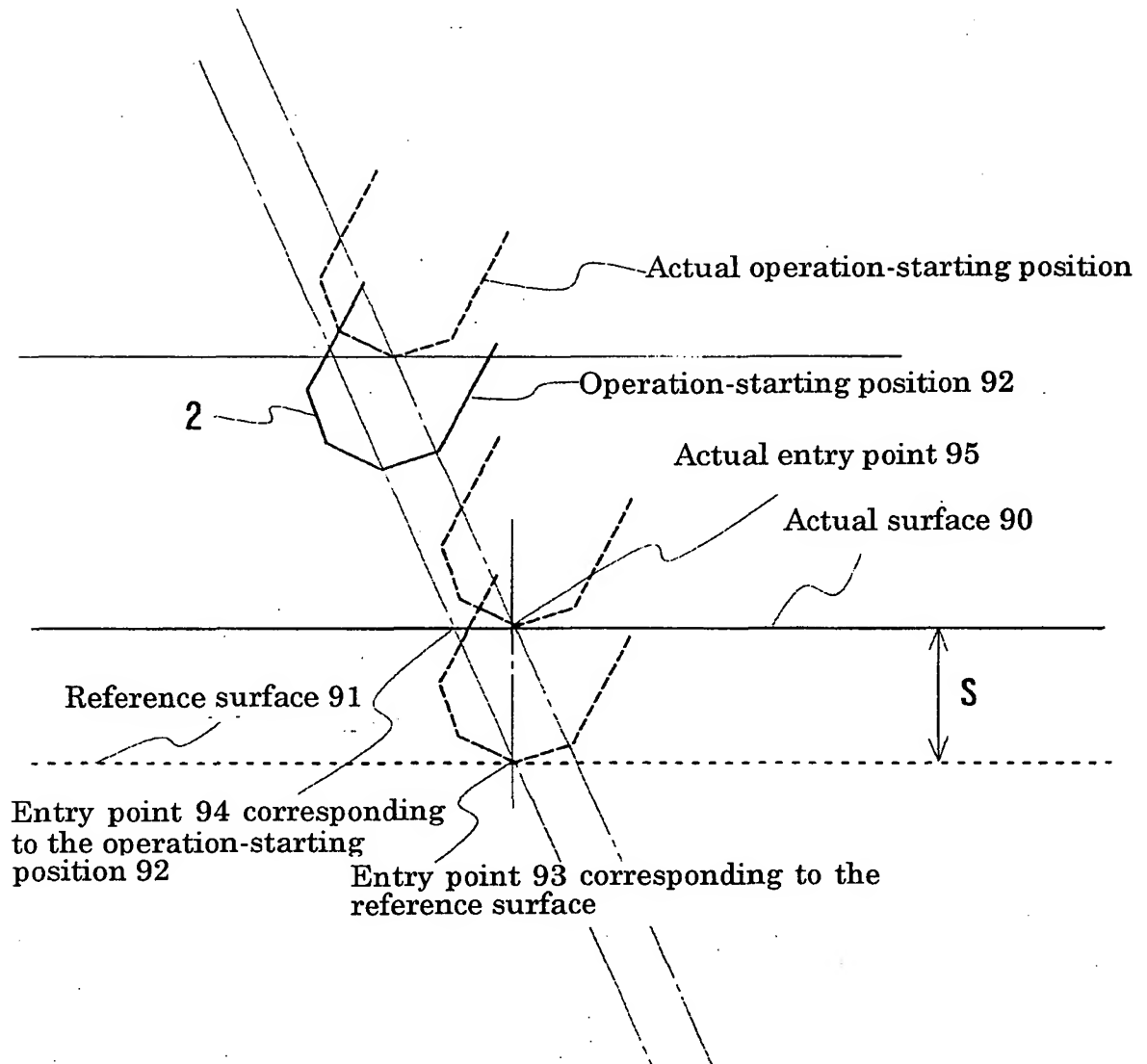


FIG. 10 (A)

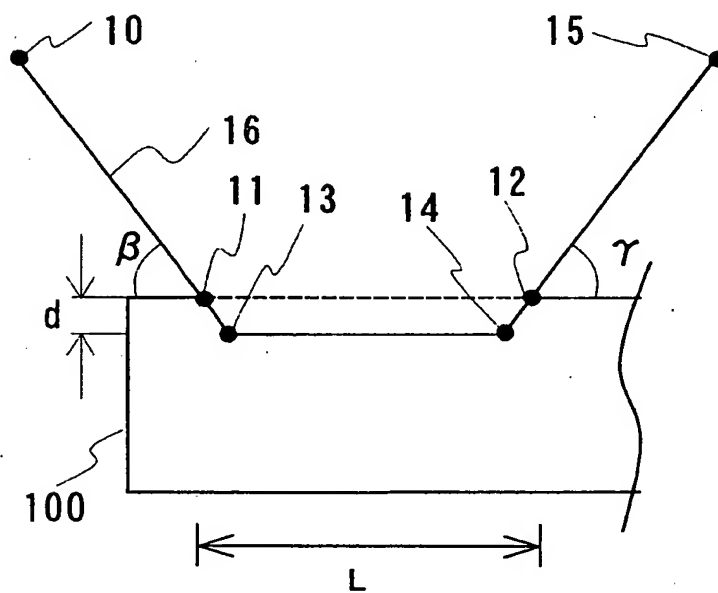


FIG. 10 (B)

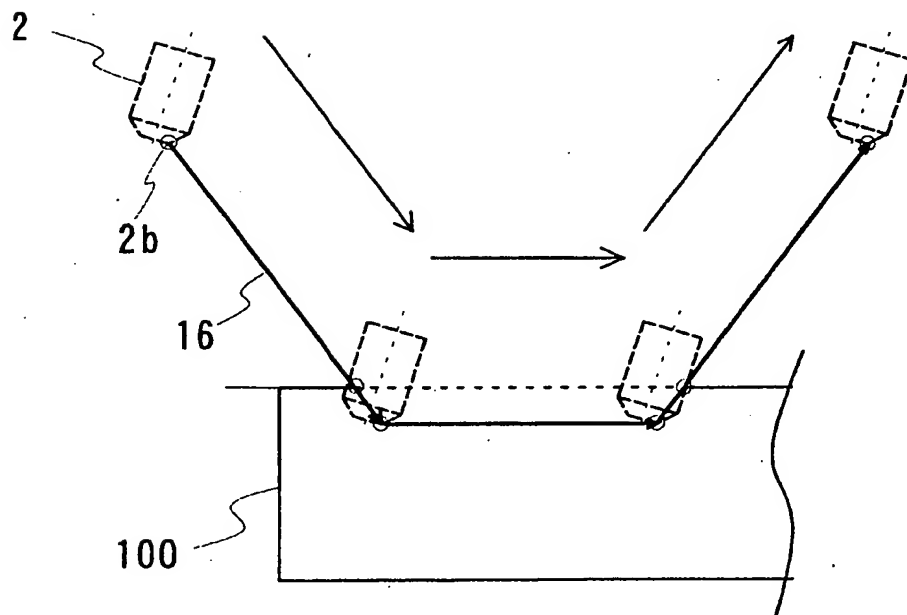


FIG. 11

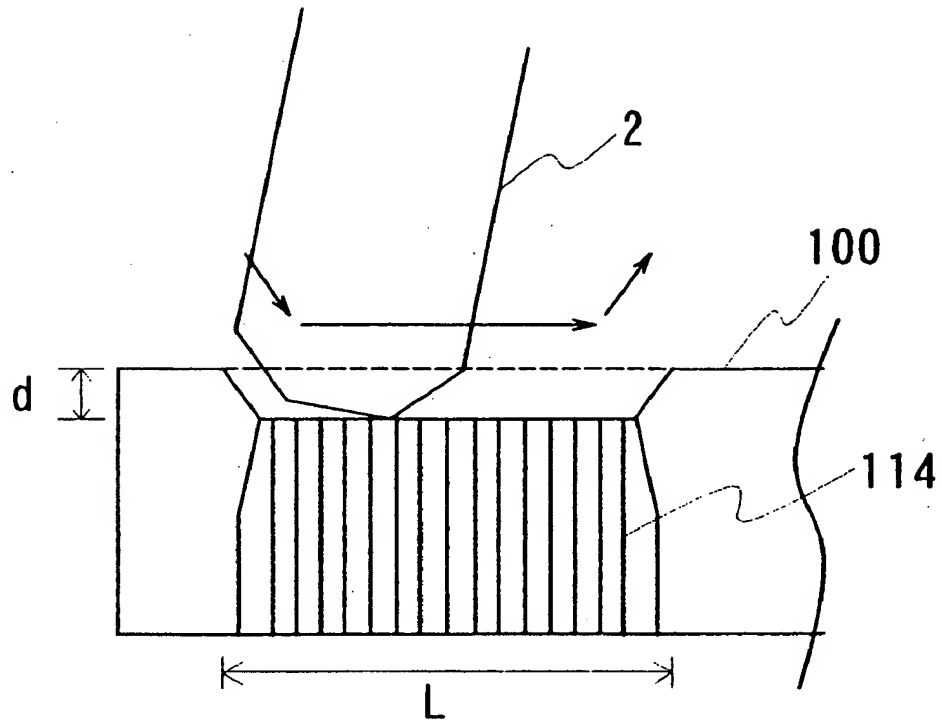


FIG. 12 (A)
Prior Art

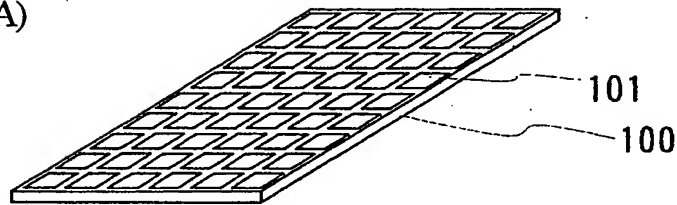


FIG. 12 (B)
Prior Art

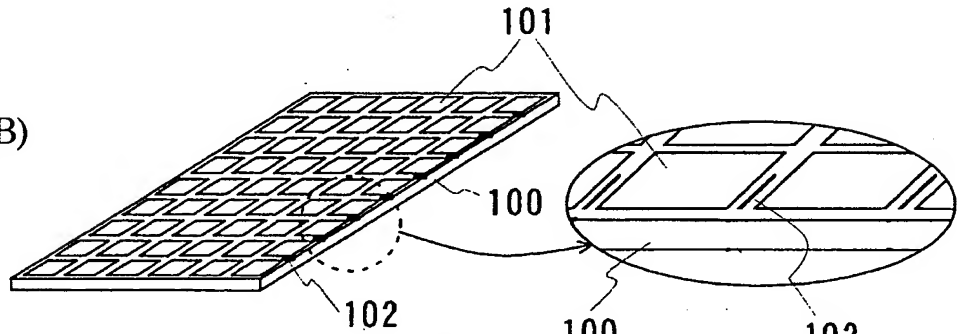


FIG. 12 (C)
Prior Art

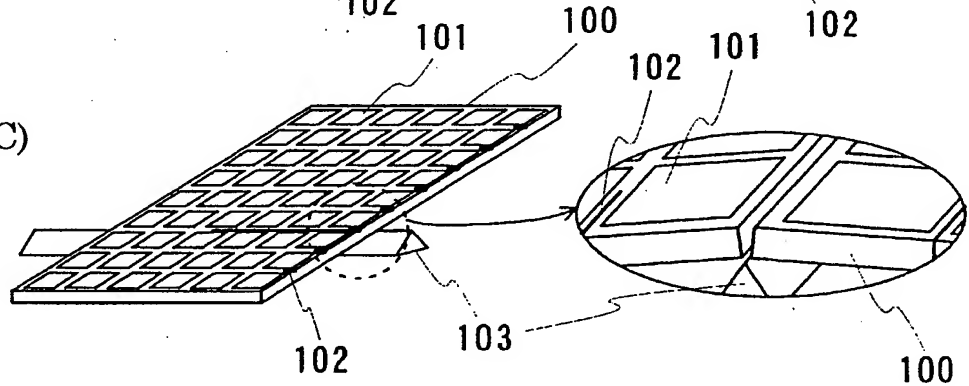


FIG. 12 (D)
Prior Art

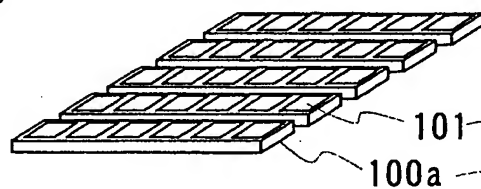


FIG. 12 (E)
Prior Art

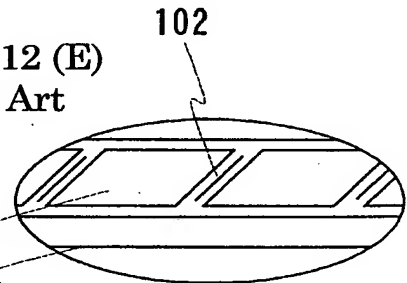


FIG. 12 (F)
Prior Art

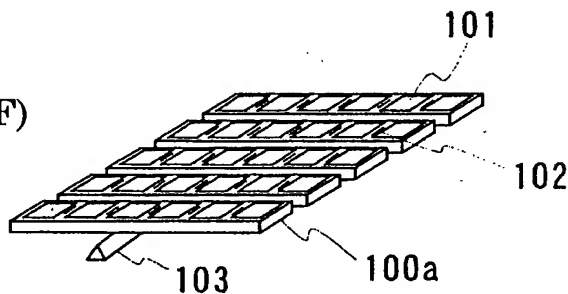


FIG. 12 (G)
Prior Art

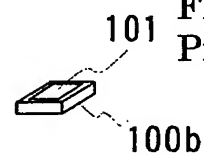


FIG. 13

Prior Art

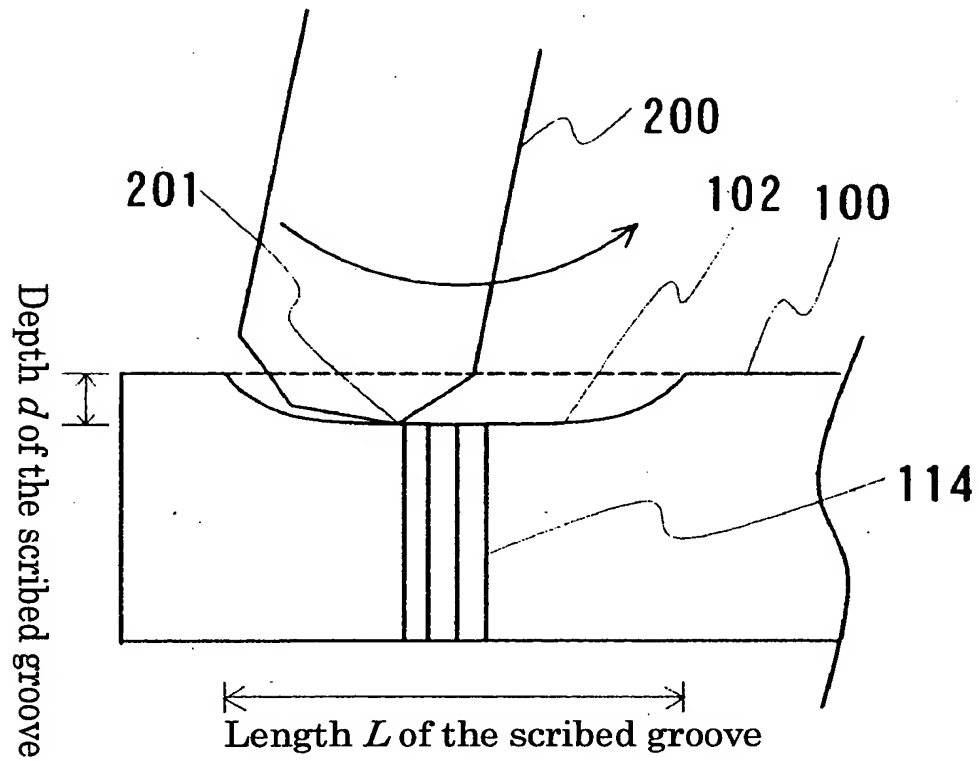
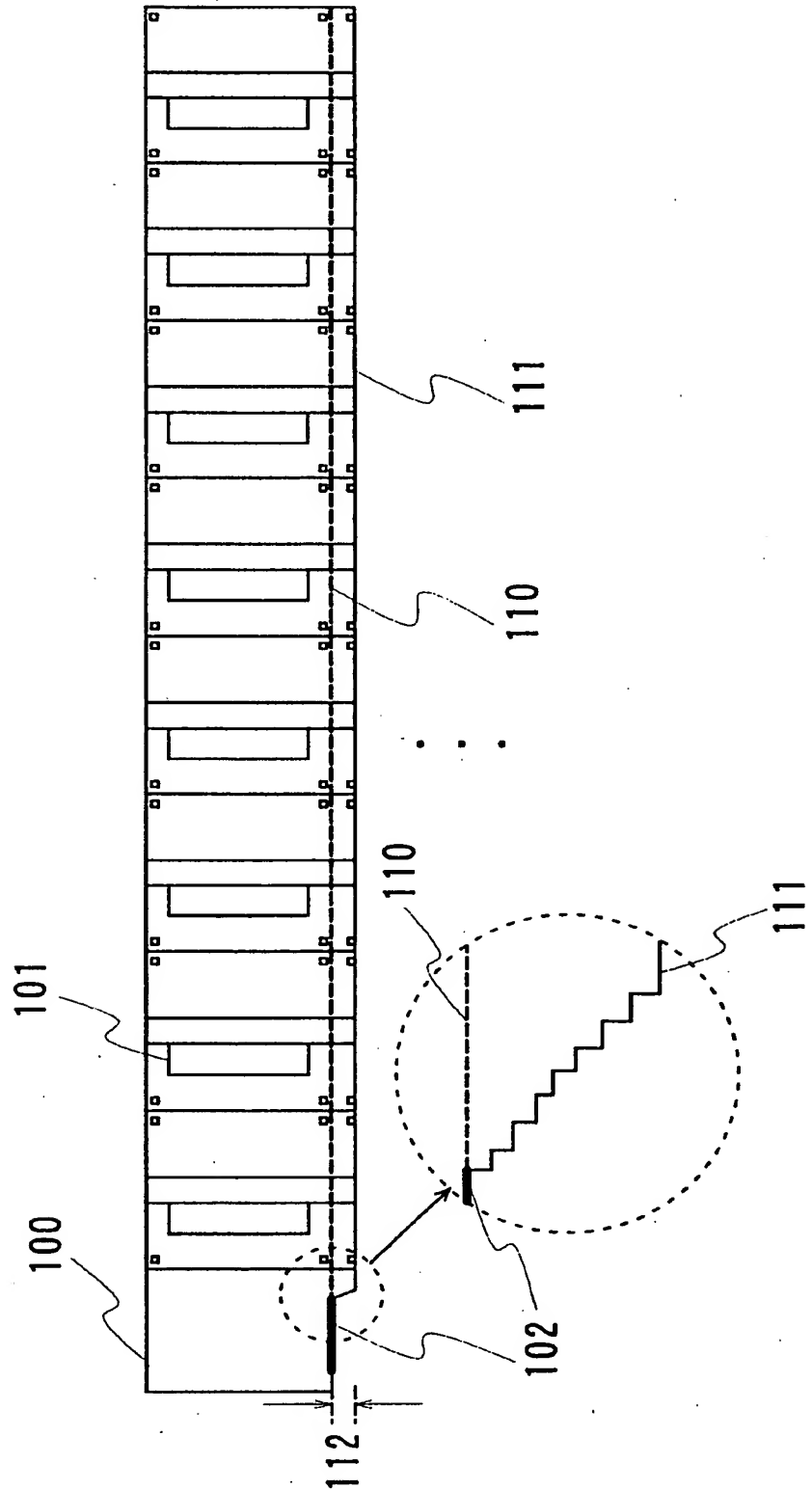


FIG. 14

Prior Art



Mounting position of the chip

FIG. 16

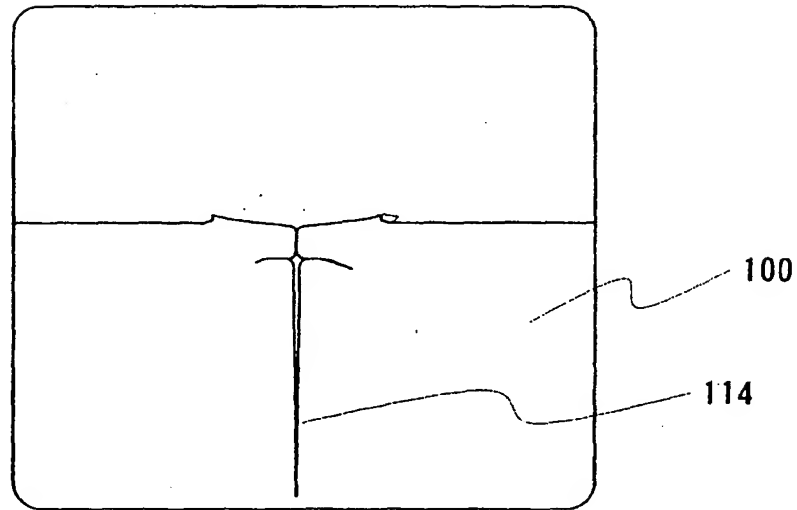


FIG. 17

Prior Art

